PATENT
Attorney Docket No. 02887.0141-01

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Yukihito OOWAKI et al.	)	Group Art Unit: 2814
	)	
Application No.: 09/879,208	)	
	)	Examiner: Shrinivas H. Rao
Filed: June 13, 2001	)	
	)	
For: MIS TRANSISTOR AND METHOD FOR PRODUCING THE SAME	)	Confirmation No.: 4453

Mail Stop Appeal Brief--Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

TRANSMITTAL OF APPEAL BRIEF (37 C.F.R. 41.37)

Transmitted herewith is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on December 11, 2006.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 C.F.R. 41.20(b)(2), the fee for filing the Appeal Brief is:

☐ $250.00 (Small Entity)

☒ $500.00 (Large Entity)

TOTAL FEE DUE:

Appeal Brief Fee	$500.00
Extension Fee (if any)	$0.00
Total Fee Due	$500.00

☒ Enclosed is a check for $500.00 to cover the above fees.

PETITION FOR EXTENSION. If any extension of time is necessary for the filing of this Appeal Brief, and such extension has not otherwise been requested, such an extension is hereby requested, and the Commissioner is authorized to charge necessary fees for such an extension to our Deposit Account No. 06-0916.

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 7, 2007

By: _____
Darrell D. Kinder, Jr.
Reg. No. 57,460

PATENT
Attorney Docket No. **02887.0141-01**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Yukihito OOWAKI et al.	Group Art Unit: 2814
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Attention: Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPEAL BRIEF UNDER RULE § 41.37

In support of the Notice of Appeal filed December 11, 2006, further to 37 C.F.R. § 41.37, Appellants present this Appeal Brief and enclose herewith a check for the fee of $500.00 required under 37 C.F.R. § 41.20(b)(2).

This Appeal is filed to appeal the rejections of claims 14-29, 31, and 32 set forth in the Final Office Action mailed September 11, 2006.

This Appeal Brief is being timely submitted within two (2) months of the December 11, 2006, filing date of the Notice of Appeal.

If any additional fees are required or if the enclosed payment is insufficient, Appellants request that the required fees be charged to Deposit Account No. 06-0916.

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I. REAL PARTY IN INTEREST

The real party in interest is Kabushiki Kaisha Toshiba, a corporation of Japan, and the assignee of the entire right, title, and interest in the application.

II. RELATED APPEALS AND INTERFERENCES

There are currently no other appeals or interferences, of which Appellants, Appellants' legal representative, or the Assignee is aware, that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 14-29, 31, and 32 are pending in the above-captioned patent application, and are the subject of this appeal.

In the Final Office Action, the Examiner rejected claims 14-29 and 31[1] under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,270,257 to Shin ("Shin") in view of U.S. Patent No. 5,949,116 to Wen ("Wen"); and rejected claim 32 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen, and further in view of U.S. Patent No. 6,228,763[2] to Lee ("Lee").

The claims on appeal are set forth in Section VIII entitled "Claims Appendix."

[1] Although on page 4 of the Office Action the Examiner indicates that claim 32 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen, Appellants believe that this is a typographical error because the Examiner indicates on page 7 of the Office Action that claim 32 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen **and further in view of Lee**.

[2] Although in the outstanding Office Action the Examiner cited U.S. Patent No. 6,248,622, attributed to Lee, Appellants believe that the Examiner meant to cite U.S. Patent No. 6,228,763 also attributed to Lee, as in previous Office Actions.

IV. STATUS OF AMENDMENTS

Appellants filed an Amendment After Final on July 22, 2005, which was entered with the Request for Continued Examination filed September 21, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 14 is directed to a method for producing a MIS transistor which comprises a semiconductor substrate, impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions. The method comprises selectively forming a first film (Fig. 3A, 9) on said semiconductor substrate (Fig. 3A, 1), and etching said semiconductor substrate to form a first groove (page 12, lines 6-12; Fig. 3B, 4) by using said first film (Fig. 3B, 9) as a mask. The method also comprises forming a second film (Fig. 3C, 10) in said first groove (Fig. 3C, 4) and thereafter removing said first film (page 12, lines 13-20; Fig. 3C, 9), and diffusing an impurity onto a surface of said semiconductor substrate (Fig. 3D, 1) using said second film (Fig. 3D, 10) as a mask to form the impurity diffusion regions (Fig. 3D, 2) including a part thereof extending below the first groove (page 12, lines 21-26; Fig. 3D, 4).

The method of claim 14 also comprises forming an insulator film (Fig. 3E, 12) on said impurity diffusion regions (Fig. 3E, 2) and thereafter removing said second film (Fig. 3E, 10) to form a second groove on the semiconductor substrate so that a top surface of each of the impurity diffusion regions (Fig. 3E, 2) of the semiconductor substrate is higher than a bottom surface of the second groove. Furthermore, the method comprises forming a gate insulator film (Fig. 3E, 5) in said second groove and controlling a thickness of the gate insulator film so that a top surface of said gate insulator film (Fig. 3E, 5) is higher than the top surface of each of said impurity diffusion

regions (Fig. 3E, 2), and forming a gate electrode (Fig. 3E, 6) on the top surface of said gate insulator film (page 12, lines 26-32; Fig. 3E, 5).

Independent claim 18 is directed to a method for producing a MIS transistor. The MIS transistor comprises a semiconductor substrate, impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions. The method for producing the MIS transistor includes selectively forming a first film (Fig. 3A, 9) on said semiconductor substrate (Fig. 3A, 1), etching said semiconductor substrate (Fig. 3B, 1) to form a first groove (page 12, lines 6-12; Fig. 3B, 4) by using said first film (Fig. 3B, 9) as a mask, and forming a second film (Fig. 3C, 10) in said first groove (Fig. 3C, 4) and thereafter removing said first film (page 12, lines 13-20; Fig. 3C, 9).

The method also includes diffusing an impurity onto a surface of said semiconductor substrate (Fig. 6B, 1) using said second film (Fig. 6B, 10) as a mask to form the impurity diffusion regions (page 15, lines 22-26; Fig. 6B, 2) including a part thereof (Fig. 6D, 2a) extending below the first groove, forming a first insulator film (Fig. 6C, 12) on said impurity diffusion regions (Fig. 6C, 2) and thereafter removing said second film (Fig. 6C, 10) to form a second groove on the semiconductor substrate so that a top surface of each of the impurity diffusion regions (Fig. 6C, 2) of the semiconductor substrate (Fig. 6C, 1) is higher than a bottom surface of the second groove, and forming a gate insulator film (Fig. 6D, 5) in said second groove and on said first insulator film (Fig. 6D, 12).

The method further includes polishing said gate insulator (Fig. 6D, 5) film by using said insulator film (Fig. 6D, 12) as a stopper and controlling a thickness of the gate insulator film (Fig. 6D, 5) so that a top surface of said gate insulator film (Fig. 6D, 5) is higher than a top surface of each of said impurity diffusion regions (page 15, lines 27-35; Fig. 6D, 2), and forming a gate electrode (Fig. 6D, 6) on the top surface of said gate insulator film (Fig. 6D, 5).

Independent claim 22 is directed to a method for producing a MIS transistor. The produced MIS transistor may include a semiconductor substrate (Fig. 4A, 1), impurity diffusion (Fig. 4B, 2) regions formed on the substrate serving as source/drain regions, and a gate electrode (Fig. 4E, 6) provided above a channel region (Fig. 4C, 7) between the source/drain regions. The method for producing this MIS transistor includes selectively forming a first film (Fig. 4A, 10) on said semiconductor substrate (Fig. 4A, 1), and diffusing an impurity onto a surface of said semiconductor substrate (Fig. 4B, 1) by using said first film (Fig. 4B, 10) as a mask (page 13, lines 10-14) to form the impurity diffusion regions (Fig. 4B, 2), including an elevated impurity diffusion region elevated above the channel region (page 13, lines 15-20; Fig. 4B, 7).

The method also includes forming an insulator film (Fig. 4C, 12) on said impurity diffusion regions (Fig. 4C, 2) so that a top surface of each of the impurity diffusion regions (Fig. 4C, 2) of the semiconductor substrate is higher than an upper level of the channel region (Fig. 4C, 7), and removing said first film (page 13, lines 21-30; Fig. 4C, 10) so as to form a groove on the semiconductor substrate. Furthermore, the method includes forming a gate insulator film (Fig. 4D, 5) in said groove on the semiconductor

substrate and controlling a thickness of the gate insulator film (Fig. 4D, 5) so that a top surface of said gate insulator film is higher than a top surface of each of said impurity diffusion regions (page 13, lines 31-33; Fig. 4D, 2), and forming a gate electrode (Fig. 4E, 6) on a top surface of said gate insulator film (page 14, lines 4-7; Fig. 4E, 5).

Independent claim 27 is directed to a method for producing a MIS transistor. The produced MIS transistor may include a semiconductor substrate (Fig. 9B, 1), impurity diffusion regions (Fig. 9E, 2a, 2b) formed on the substrate serving as source/drain regions, and a gate electrode (page 17, lines 9-17; Fig. 9C, 6) provided above a channel region between the source/drain regions. The method for producing the MIS transistor includes sequentially depositing on the semiconductor substrate (Fig. 9B, 1) a high dielectric film (Fig. 9B, 5) to serve as a gate insulator film and a polycrystalline semiconductor film (page 17, lines 13-15; Fig. 9B, 6) to serve as a gate electrode, to form a laminate structure, and etching said laminate structure so as to form said gate electrode (Fig. 9C, 6) and thereafter forming side walls (Fig. 9D, 8) on sides of said gate electrode (page 17, lines 17-21; Fig. 9D, 6).

The claimed method also includes etching said high dielectric film (Fig. 9E, 5) so as to form said gate insulator film (Fig. 9E, 5) by using said gate electrode (Fig. 9E, 6) and side walls (Fig. 9E, 8) as a mask and forming a side wall insulator film (Fig. 9E, 3b) at a side of said gate insulator film (page 17, lines 22-25; Fig. 9E, 5), and diffusing an impurity onto a surface of said semiconductor substrate to form the impurity diffusion regions (page 17, lines 27-28; Fig. 9E, 2a, 2b) including an elevated impurity diffusion region (Fig. 9E, 2b) elevated from a channel region (page 17, line 26; Fig. 9E, 7) and

controlling a thickness of the elevated impurity diffusion region (Fig. 9E, 2b) by using said gate insulator film (Fig. 9E, 5) as a mask, so that a top surface of the gate insulator film (Fig. 9E, 5) is higher than a top surface of the elevated impurity diffusion region (Fig. 9E, 2b) and that said top surface of the elevated impurity diffusion region (Fig. 9E, 2b) is higher than a top surface of said channel region (page 17, lines 27-36; Fig. 9E, 7) of the semiconductor substrate.

Independent claim 32 is also directed to a method for producing a MIS transistor. The produced MIS transistor may include a semiconductor substrate, source/drain regions (Fig. 13A, 104) formed on the substrate, and a gate electrode (Fig. 13D, 114) provided above a channel region between the source/drain regions. The method for producing the MIS transistor includes forming a dummy film (Fig. 13A, 101) on said channel region, which borders said source/drain regions (page 21, lines 14-16; Fig. 13A, 104), and selectively depositing semiconductor layers (Fig. 13A, 104) serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor layers (page 21, lines 31-37; Fig. 13A, 104) and said channel region.

The method further includes diffusing an impurity onto a surface of said semiconductor substrate (Fig. 13A, 105) to form impurity diffusion regions (Fig. 13A, 110) by using said dummy film (page 22, lines 21-24; Fig. 13A, 101) as a mask and thereafter removing said dummy film (page 24, lines 16-19; Fig. 13A, 101), depositing an insulator film (Fig. 13D, 113) on an exposed surface of said channel region to form a gate insulator film (page 24, lines 29-32; Fig. 13D, 113), which has a cross section of a

grooved space at a center thereof; and depositing a gate electrode (Fig. 13D, 114) on a top of said gate insulator film (page 25, lines 1-4; Fig. 13D, 113) to form a gate electrode having a cross section of a T shape.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 14-29 and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen.

2. Claim 32 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen, and further in view of Lee.

VII. ARGUMENT

A. Introduction

Each claim of this patent application is separately patentable and, upon issuance of a patent, will be entitled to a separate presumption of validity under 35 U.S.C. § 282. That is, each of claims 14-29, 30, and 31 should be considered individually in light of the arguments against the Examiner's rejections.

B. Detailed Arguments

1. The rejection of claims 14-29 and 31 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen should be reversed.

The rejection of claims 14-29 and 31 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen should be reversed because no *prima facie* case of obviousness has been established.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." *See* MPEP § 2143, 8th Ed. (Rev. 5), August, 2006.

At least the first essential element for establishing a *prima facie* case of obviousness has not been met. Specifically, neither Shin nor Wen, whether taken alone or in combination, teach or suggest every element recited in claims 14-29 and 31.

A. Claims 14-21

Regarding the Examiner's rejection of independent claims 14 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen, each of independent claims 14 and 18 recites a combination including "removing said second film to form a second groove on the semiconductor substrate ... [and] forming a gate insulator film in said second groove." Shin and Wen, whether taken alone or in combination, fail to teach or suggest at least this element.

In the Final Office Action, the Examiner acknowledges that Shin fails to teach or suggest at least this element, stating: "Shin does not specifically disclose the steps of ... removing said second film to form a second groove in the semiconductor substrate." Final Office Action, page 4. Therefore, by the Examiner's own admission, Shin fails to provide the necessary disclosure to constitute a teaching of "removing said second film to form a second groove on the semiconductor substrate ... [and] forming a gate insulator film in said second groove." as recited in independent claims 14 and 18.

To attempt to cure the deficiencies of Shin, the Examiner cites Wen asserting that Wen teaches "removing the second film to form a second groove on the semiconductor substrate (Figure 2C removal of 201, 207) so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than a bottom surface of the second groove, (figure 2C 200 above 209)." Id., at page 5. The Examiner has

thus apparently characterized elements 201 and 207 of Wen as constituting Appellants' claimed "second film." Elements 201 and 207 are allegedly removed to form element 209 of Figure 2C, which the Examiner has characterized as constituting Appellants' claimed "second groove." Even if the Examiner's characterization could be considered correct, Appellants note that the Examiner further asserts that Wen teaches "forming a gate insulator film in said second groove" at element "21"[3] in Figs. 2D to 2F. *See* Final Office Action, page 5. That is, the Examiner has apparently construed Wen as teaching removing elements 201 and 207 to form a second groove 209, and then forming gate insulator film 210 in the formed second groove 209.

Appellants disagree with the Examiner's characterization of Wen. However, even if the Examiner's characterization could be considered correct, Appellants initially note that element 210 is an insulating layer which is separate from, and not part of, the gate structure including elements 203 and 204. *See* Wen, col. 3, lines 23-24. Moreover, since element 210 of Wen is formed outside of the region beneath gate 204, and not between the source and drain regions, element 210 cannot act as or constitute a portion of a gate structure. Accordingly, element 210 of Wen cannot constitute "a gate insulator film" formed in a second groove, as characterized by the Examiner. Wen thus cannot teach or suggest "removing said second film to form a second groove on the semiconductor substrate ... [and] forming a gate insulator film in said second groove," as recited in independent claims 14 and 18 (emphasis added). Wen therefore cannot cure the above-noted deficiencies of Shin.

[3] Appellants note that Wen does not contain an element **"21"** in Figs. 2D to 2F. Appellants assume that the Examiner is actually referring to element **210** in Figs 2D-2F of Wen.

The Examiner has therefore not met an essential element for establishing a *prima facie* case of obviousness, specifically, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations." *See* MPEP §§ 2142, 2143, and 2143.03. Since establishing a *prima facie* case of obviousness requires that the cited reference or references teach or suggest each and every element of the claimed invention, the Examiner's 35 U.S.C. § 103(a) rejection fails on at least this point.

Moreover, Appellant further notes that "[i]n determining the differences between the prior art and the claims, the question under 35 U.S.C. § 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. MPEP § 2141.02 (*citing* Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); Schenck v. Nortron Corp., 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983)). Here, the Examiner has not shown that independent claims 14 and 18, when viewed as a whole, would have been obvious over Shin in view of Wen. For at least these additional reasons, *prima facie* obviousness of independent claims 14 and 18 has not been established.

Because no *prima facie* case of obviousness of independent claims 14 and 18 has been established, these independent claims are therefore allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596 (Fed. Cir. 1988). Dependent claims 15-17 and claims 19-21 are therefore also allowable at least by virtue of their respective dependency from allowable independent claims 14 and 18.

Therefore, the improper rejection of claims 14-21 under 35 U.S.C. § 103(a) should be reversed.

B. Claims 22-26

Regarding the Examiner's rejection of independent claim 22 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen, independent claim 22 recites a combination including "controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region." Shin or Wen, whether taken alone or in combination, fail to teach or suggest at least this element.

In the Final Office Action, the Examiner alleges that "[c]laim 22 repeats the steps of claim 18 except for the absence of the second film-forming step and is rejected for reasons stated under claim 18 above." Final Office Action, page 6. Accordingly, because the Examiner is apparently applying the same rejection as above with respect to independent claim 18 (and independent claim 14), the Examiner also apparently acknowledges that Shin fails to provide the disclosure necessary to teach or suggest a combination including "forming a gate insulator film in said groove," as discussed, *supra*, with respect to independent claims 14 and 18.

For similar reasons as given *supra* with respect to independent claims 14 and 18, Wen cannot cure this deficiency. The Examiner alleges that element [210] of Wen as shown in Figs. 2D to 2F constitutes a gate insulating layer. Final Office Action, page 5. For reasons similar to those given above in the discussion of independent claims 14 and 18, element 210 of Wen **cannot** constitute a portion of or act as a gate structure.

Moreover, Appellants note that *even if* insulator 210 of Wen could be reasonably construed to constitute Appellants' claimed "gate insulator film," element 210 is formed such that the top surface of 210, as shown in Fig. 2D of Wen, is below a top surface of the impurity diffusion region 217. *See* Wen col. 3, lines 23-27, and Fig. 3. Accordingly, Wen fails to teach or suggest "controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region," (emphasis added) as recited in independent claim 22. Wen thus cannot cure the above-noted deficiencies of Shin.

The Examiner has therefore not met an essential element for establishing a *prima facie* case of obviousness, specifically, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations." *See* MPEP §§ 2142, 2143, and 2143.03. Since establishing a *prima facie* case of obviousness requires that the cited reference or references teach or suggest each and every element of the claimed invention, the Examiner's 35 U.S.C. § 103(a) rejection fails on at least this point.

Because no *prima facie* case of obviousness of independent claim 22 has been established, this independent claim is therefore allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596 (Fed. Cir. 1988). Dependent claims 23-26 are therefore also allowable at least by virtue of their respective dependency from allowable independent claim 22. Therefore, the improper rejection of claims 22-26 under 35 U.S.C. § 103(a) should be reversed.

C. Claims 27-29 and 31

Regarding the rejection of independent claim 27 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen, claim 27 recites a combination including "sequentially depositing on the semiconductor substrate a high dielectric film to serve as a gate insulator film and a polycrystalline semiconductor film to serve as a gate electrode, to form a laminate structure." Shin and Wen, whether taken alone or in combination, fail to teach or suggest at least this element.

Shin teaches "a nitride layer 22 is first deposited on a silicon substrate ... [and] is then subjected to a photo lithography process, to etch the portion thereof positioned as the region where a gate is to be formed." Shin, col. 4, lines 20-23 (emphasis added). Shin then teaches "a gate oxide layer 23 is grown on the overall exposed trench surface ... [and] a polysilicon layer 24 is thickly deposited to fill the trench of silicon substrate." Id., at col. 4, lines 30-37. Shin thus teaches depositing nitride layer 22, etching nitride layer 22, forming gate oxide layer 23, then forming polysilicon layer 24.

To the extent that gate oxide layer 23 can be reasonably construed as corresponding to Appellants' claimed "gate insulator film," Shin fails to provide a teaching or suggestion that a high dielectric film serves as gate oxide film 23. In fact, Shin provides no teaching that gate oxide film 23 or any of the other films are high dielectric films. Accordingly, Shin fails to teach or suggest a combination including "sequentially depositing on the semiconductor substrate a high dielectric film to serve as a gate insulator film and a polycrystalline semiconductor film to serve as a gate

electrode, to form a laminate structure," as recited in independent claim 27 (emphasis added).

Wen fails to cure the above noted deficiency of Shin. Wen teaches "an insulating layer is formed, for example, by thermal oxidation, to provide a field oxide with a bird's beak structure ... followed by the formation of a gate oxide layer 203 and a gate 204, in order, on the substrate." Wen, col. 2, lines 31-37. Wen, however, provides no teaching that any of the formed insulating layers are high dielectric films. Wen thus fails to provide a teaching or suggestion of "sequentially depositing on the semiconductor substrate a high dielectric film to serve as a gate insulator film and a polycrystalline semiconductor film to serve as a gate electrode, to form a laminate structure," as recited in independent claim 27 (emphasis added). Wen therefore cannot cure the deficiencies of Shin.

The Examiner has therefore not met an essential element for establishing a *prima facie* case of obviousness, specifically, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations." *See* MPEP §§ 2142, 2143, and 2143.03. Since establishing a *prima facie* case of obviousness requires that the cited reference or references teach or suggest each and every element of the claimed invention, the Examiner's 35 U.S.C. § 103(a) rejection fails on at least this point.

Because no *prima facie* case of obviousness of independent claim 27 has been established, this independent claim is therefore allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious.

In re Fine, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596 (Fed. Cir. 1988). Dependent claims 28, 29, and 31 are therefore also allowable at least by virtue of their respective dependency from allowable independent claim 27. Therefore, the improper rejection of claims 27-29, and 31 under 35 U.S.C. § 103(a) should be reversed.

2. The rejection of independent claim 32 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen and further in view of Lee should be reversed.

Regarding the Examiner's rejection of independent claim 32 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Wen and further in view of Lee, at least the first essential element (listed in section 1, *supra*) for establishing a *prima facie* case of obviousness has not been met. Specifically, neither Shin nor Wen nor Lee, whether taken alone or in combination, teach or suggest every element recited in claim 32. For example, claim 32 recites a combination including "selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor layers and said channel region." Shin, Wen, and Lee, whether taken alone or in combination, fail to teach or suggest at least this element of independent claim 32.

Shin teaches the formation of source/drain regions 26a, b and 28a, b (Fig. 3e) on top of semiconductor substrate 21 (as shown in Fig. 3a). *See* Shin, col. 4 ,line 63 - col. 5, line 3. From Fig. 3e, it appears that a surface of source 26a and drain 26b is inclined. However, independent claim 32 recites "an inclined surface is formed between the top surface of said semiconductor layers and said channel region" (emphasis added). As shown in Fig. 3e of Shin, the "top surface" of the semiconductors layers is a top surface of source 28a and drain 28b, which are on top of source 26a and drain 26b,

respectively. Accordingly, even if a surface of source 26a and drain 26b could reasonably be construed as being "inclined," the surface of source 26a and drain 26b are not "the top surface of said semiconductor layers," as recited in independent claim 32. Shin therefore fails to teach or suggest a combination including "selectively depositing semiconductor layers ... so that an inclined surface is formed between the top surface of said semiconductor layers and said channel region," as recited in independent claim 32 (emphasis added).

Wen fails to cure the above-noted deficiencies of Shin. Wen teaches "form[ing] a gate oxide layer 203 and a gate 204, in order, on a substrate 205." Wen, col. 2, lines 36-37. To the extent that the region beneath gate oxide layer 23 corresponds to Appellants' claimed "channel region," Wen shows, in Fig. 2E, diffusion regions 200 and 217 which appear to be at a top surface of substrate 205. However, Wen fails to show "an inclined surface" between these regions and the region beneath gate oxide layer 203. Wen thus fails to teach or suggest a combination including "selectively depositing semiconductor layers ... so that an inclined surface is formed between the top surface of said semiconductor layers and said channel region," as recited in independent claim 32 (emphasis added). Wen therefore cannot be relied upon to cure the above-noted deficiencies of Shin.

Lee also cannot cure the above-noted deficiencies of Shin and Wen. The Examiner cites Lee for allegedly teaching "a metal layer and a damascene structure that has a T-shaped cross-section." Final Office Action, pages 7-8. Although Appellants do not necessarily agree with the Examiner's assertion, the Examiner has not asserted that

Lee teaches "selectively depositing semiconductor layers ... so that an inclined surface is formed between the top surface of said semiconductor layers and said channel region," as recited in independent claim 32. Indeed, Lee provides no such teaching. Accordingly, Lee cannot cure the above-noted deficiencies of Shin and Wen.

The Examiner has therefore not met an essential element for establishing a *prima facie* case of obviousness, specifically, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations." *See* MPEP §§ 2142, 2143, and 2143.03. Since establishing a *prima facie* case of obviousness requires that the cited references teach or suggest each and every element of the claimed invention, the Examiner's 35 U.S.C. § 103(a) rejection fails on at least this point.

Because no *prima facie* case of obviousness of independent claim 32 has been established, independent claim 32 is therefore allowable.

For the reasons given above, pending claims 14-29, 31, and 32 are allowable. Appellants respectfully request that the Board reverse the Examiner's rejections.

To the extent any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Appeal Brief, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 that are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 7, 2007

By: _____
Darrell D. Kinder, Jr.
Reg. No. 57,460

VIII. CLAIMS APPENDIX

Claims Appendix to Appeal Brief Under Rule 41.37(c)(1)(viii)

14. A method for producing a MIS transistor comprising a semiconductor substrate, impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity onto a surface of said semiconductor substrate using said second film as a mask to form the impurity diffusion regions including a part thereof extending below the first groove;

forming an insulator film on said impurity diffusion regions and thereafter removing said second film to form a second groove on the semiconductor substrate so that a top surface of each of the impurity diffusion regions of the semiconductor substrate is higher than a bottom surface of the second groove;

forming a gate insulator film in said second groove and controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than the top surface of each of said impurity diffusion regions; and

forming a gate electrode on the top surface of said gate insulator film.

15. A method for producing a MIS transistor according to claim 14, wherein said second film is a semiconductor film, and further comprising:

forming a sacrificial film in said first groove before forming said second film in said first groove; and

removing said sacrificial film after removing said second film to form said second groove.

16. A method for producing a MIS transistor according to claim 14, further comprising:

polishing a surface of said second film by using said first film as a stopper.

17. A method for producing a MIS transistor according to claim 14, further comprising:

forming a protective film in said second groove before forming said gate insulator film in said second groove.

18. A method for producing a MIS transistor comprising a semiconductor substrate, impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity onto a surface of said semiconductor substrate using said second film as a mask to form the impurity diffusion regions including a part thereof extending below the first groove;

forming a first insulator film on said impurity diffusion regions and thereafter removing said second film to form a second groove on the semiconductor substrate so that a top surface of each of the impurity diffusion regions of the semiconductor substrate is higher than a bottom surface of the second groove;

forming a gate insulator film in said second groove and on said first insulator film;

polishing said gate insulator film by using said insulator film as a stopper and controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of each of said impurity diffusion regions; and

forming a gate electrode on the top surface of said gate insulator film.

19. A method for producing a MIS transistor according to claim 18, wherein said second film is a semiconductor film, and further comprising:

forming a sacrificial film in said first groove before forming said second film in said first groove; and

removing said sacrificial film after removing said second film to form said second groove.

20. A method for producing a MIS transistor according to claim 18, further comprising:

polishing a surface of said second film by using said first film as a stopper.

21. A method for producing a MIS transistor according to claim 18, further comprising:

forming a protective film in said second groove before forming said gate insulator film in said second groove.

22. A method for producing a MIS transistor comprising a semiconductor substrate, impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

diffusing an impurity onto a surface of said semiconductor substrate by using said first film as a mask to form the impurity diffusion regions, including an elevated impurity diffusion region elevated above the channel region;

forming an insulator film on said impurity diffusion regions so that a top surface of each of the impurity diffusion regions of the semiconductor substrate is higher than an upper level of the channel region;

removing said first film so as to form a groove on the semiconductor substrate;

forming a gate insulator film in said groove on the semiconductor substrate and controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of each of said impurity diffusion regions; and

forming a gate electrode on a top surface of said gate insulator film.

23. A method for producing a MIS transistor according to claim 22, further comprising:

elevating said elevated impurity diffusion region by an epitaxial growth technique before diffusing said impurity onto said surface of said semiconductor substrate .

24. A method for producing a MIS transistor according to claim 22, further comprising:

diffusing an impurity on said surface of said semiconductor substrate before elevating said elevated impurity diffusion region by an epitaxial growth technique.

25. A method for producing a MIS transistor according to claim 22, wherein said first film is semiconductor film and further comprising:

forming a sacrificial film on a surface of said first film; and

removing said sacrificial film.

26. A method for producing a MIS transistor according to claim 22, further comprising:

forming a protective film in said groove before forming said gate insulator film in said groove.

27. A method for producing a MIS transistor comprising a semiconductor substrate, impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

sequentially depositing on the semiconductor substrate a high dielectric film to serve as a gate insulator film and a polycrystalline semiconductor film to serve as a gate electrode, to form a laminate structure;

etching said laminate structure so as to form said gate electrode and thereafter forming side walls on sides of said gate electrode;

etching said high dielectric film so as to form said gate insulator film by using said gate electrode and side walls as a mask and forming a side wall insulator film at a side of said gate insulator film; and

diffusing an impurity onto a surface of said semiconductor substrate to form the impurity diffusion regions including an elevated impurity diffusion region elevated from a channel region and controlling a thickness of the elevated impurity diffusion region by using said gate insulator film as a mask, so that a top surface of the gate insulator film is higher than a top surface of the elevated impurity diffusion region and that said top

surface of the elevated impurity diffusion region is higher than a top surface of said channel region of the semiconductor substrate.

28. A method for producing a MIS transistor according to claim 27, further comprising:

elevating said elevated impurity diffusion region by an epitaxial growth technique before diffusing said impurity on said surface of said semiconductor substrate.

29. A method for producing a MIS transistor according to claim 27, further comprising:

diffusing an impurity on said surface of said semiconductor substrate before elevating said elevated impurity diffusion region by the epitaxial growth technique.

31. A method for producing a MIS transistor according to claim 27, further comprising:

forming a protective film on the semiconductor substrate before forming said gate insulator film on the semiconductor substrate.

32. A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

forming a dummy film on said channel region, which borders said source/drain regions;

selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor layers and said channel region;

diffusing an impurity onto a surface of said semiconductor substrate to form impurity diffusion regions by using said dummy film as a mask and thereafter removing said dummy film;

depositing an insulator film on an exposed surface of said channel region to form a gate insulator film, which has a cross section of a grooved space at a center thereof; and

depositing a gate electrode on a top of said gate insulator film to form a gate electrode having a cross section of a T shape.

IX. EVIDENCE APPENDIX

NONE

X. RELATED PROCEEDINGS APPENDIX

NONE